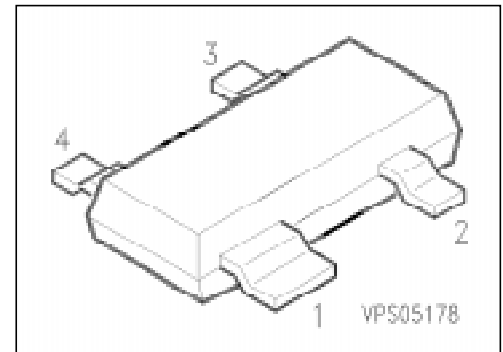


Features

- Short-channel transistor with high S/C quality factor
- For low-noise, gain-controlled input stages up to 1 GHz



Type	Marking	Ordering Code (tape and reel)	Pin Configuration				Package ¹⁾
			1	2	3	4	
BF 998	MO	Q62702-F1129	S	D	G ₂	G ₁	SOT-143

Maximum Ratings

Parameter	Symbol	Values	Unit
Drain-source voltage	V_{DS}	12	V
Drain current	I_D	30	mA
Gate 1/gate 2 peak source current	$\pm I_{G1/2SM}$	10	
Total power dissipation, $T_s < 76\text{ °C}$	P_{tot}	200	mW
Storage temperature range	T_{stg}	- 55 ... + 150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

Junction - soldering point	$R_{th JS}$	< 370	K/W
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¹⁾ For detailed information see chapter Package Outlines.

Electrical Characteristics

at $T_A = 25\text{ °C}$, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

DC Characteristics

Drain-source breakdown voltage $I_D = 10\ \mu\text{A}$, $-V_{G1S} = -V_{G2S} = 4\ \text{V}$	$V_{(BR)DS}$	12	–	–	V
Gate 1-source breakdown voltage $\pm I_{G1S} = 10\ \text{mA}$, $V_{G2S} = V_{DS} = 0$	$\pm V_{(BR)G1SS}$	8	–	12	
Gate 2-source breakdown voltage $\pm I_{G2S} = 10\ \text{mA}$, $V_{G1S} = V_{DS} = 0$	$\pm V_{(BR)G2SS}$	8	–	12	
Gate 1-source leakage current $\pm V_{G1S} = 5\ \text{V}$, $V_{G2S} = V_{DS} = 0$	$\pm I_{G1SS}$	–	–	50	nA
Gate 2-source leakage current $\pm V_{G2S} = 5\ \text{V}$, $V_{G1S} = V_{DS} = 0$	$\pm I_{G2SS}$	–	–	50	
Drain current $V_{DS} = 8\ \text{V}$, $V_{G1S} = 0$, $V_{G2S} = 4\ \text{V}$	I_{DSS}	2	–	18	mA
Gate 1-source pinch-off voltage $V_{DS} = 8\ \text{V}$, $V_{G2S} = 4\ \text{V}$, $I_D = 20\ \mu\text{A}$	$-V_{G1S(p)}$	–	–	2.5	V
Gate 2-source pinch-off voltage $V_{DS} = 8\ \text{V}$, $V_{G1S} = 0$, $I_D = 20\ \mu\text{A}$	$-V_{G2S(p)}$	–	–	2	

Electrical Characteristics

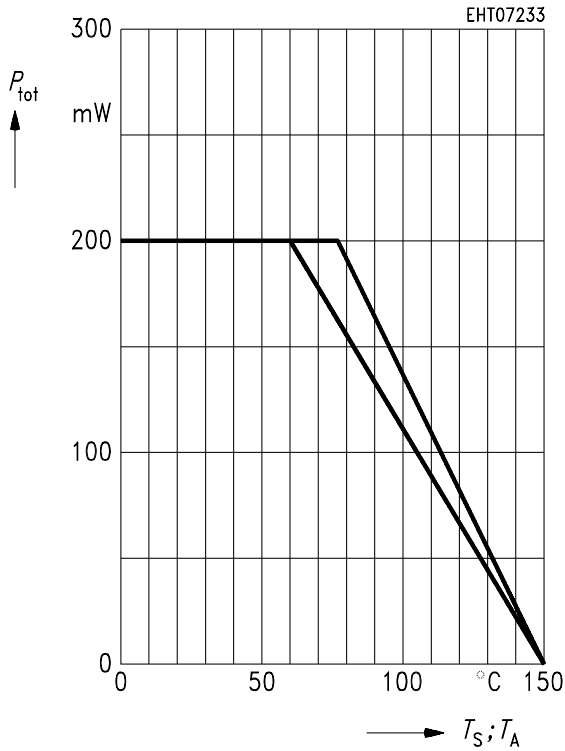
at $T_A = 25\text{ °C}$, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

AC Characteristics

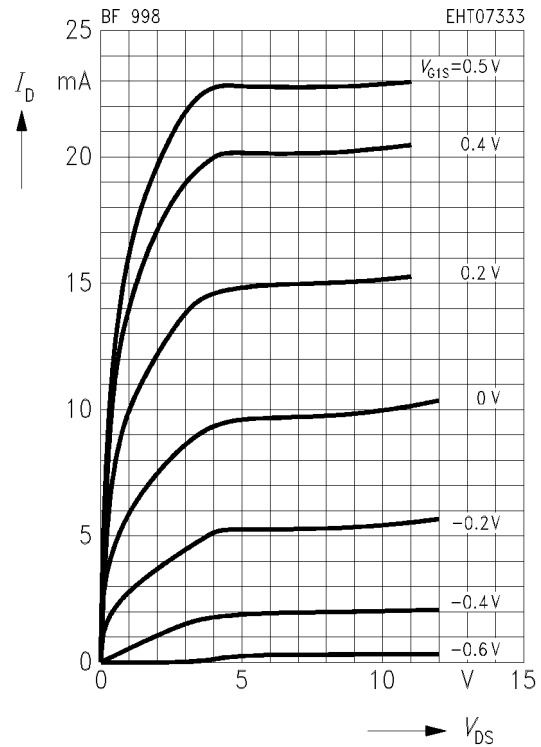
Forward transconductance $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$ $f = 1\text{ kHz}$	g_{fs}	–	24	–	mS
Gate 1 input capacitance $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$ $f = 1\text{ MHz}$	C_{g1ss}	–	2.1	2.5	pF
Gate 2 input capacitance $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$ $f = 1\text{ MHz}$	C_{g2ss}	–	1.2	–	
Reverse transfer capacitance $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$ $f = 1\text{ MHz}$	C_{dg1}	–	25	–	fF
Output capacitance $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $V_{G2S} = 4\text{ V}$ $f = 1\text{ MHz}$	C_{dss}	–	1.05	–	pF
Power gain (test circuit 1) $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$, $G_G = 2\text{ mS}$, $G_L = 0.5\text{ mS}$, $V_{G2S} = 4\text{ V}$	G_{ps}	–	28	–	dB
Power gain (test circuit 2) $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $f = 800\text{ MHz}$, $G_G = 3.3\text{ mS}$, $G_L = 1\text{ mS}$, $V_{G2S} = 4\text{ V}$	G_{ps}	–	20	–	
Noise figure (test circuit 1) $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $f = 200\text{ MHz}$, $G_G = 2\text{ mS}$, $G_L = 0.5\text{ mS}$, $V_{G2S} = 4\text{ V}$	F	–	0.6	–	dB
Noise figure (test circuit 2) $V_{DS} = 8\text{ V}$, $I_D = 10\text{ mA}$, $f = 800\text{ MHz}$, $G_G = 3.3\text{ mS}$, $G_L = 1\text{ mS}$, $V_{G2S} = 4\text{ V}$	F	–	1	–	
Control range (test circuit 2) $V_{DS} = 8\text{ V}$, $V_{G2S} = 4 \dots - 2\text{ V}$ $f = 800\text{ MHz}$	ΔG_{ps}	40	–	–	

Total power dissipation $P_{tot} = f(T_A)$



Output characteristics $I_D = f(V_{DS})$

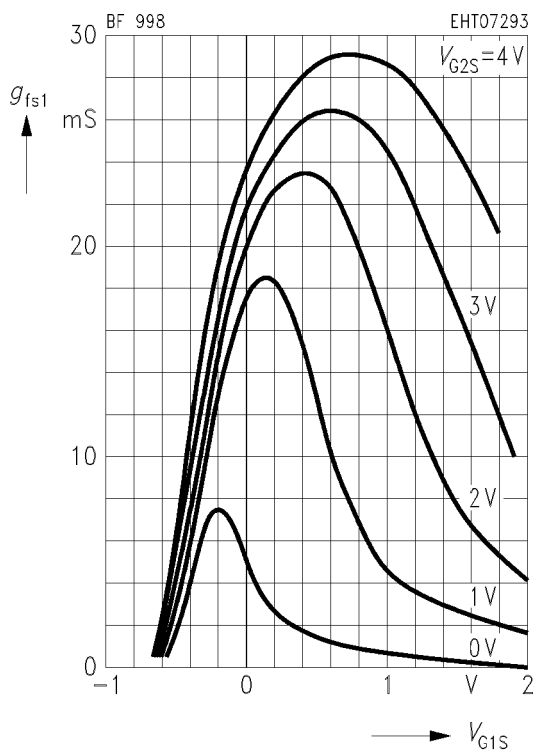
$V_{G2S} = 4 \text{ V}$



Gate 1 forward transconductance $g_{fs1} = f(V_{G1S})$

$g_{fs1} = f(V_{G1S})$

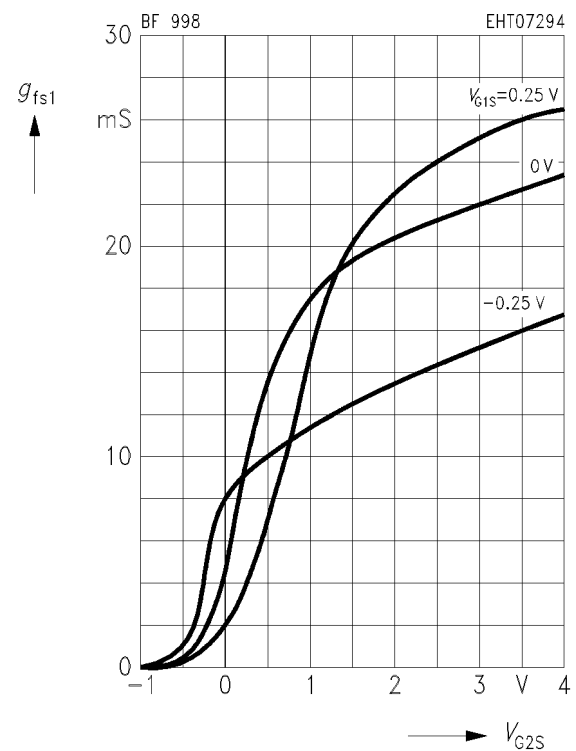
$V_{DS} = 8 \text{ V}, I_{DSS} = 10 \text{ mA}, f = 1 \text{ kHz}$



Gate 1 forward transconductance $g_{fs1} = f(V_{G2S})$

$g_{fs1} = f(V_{G2S})$

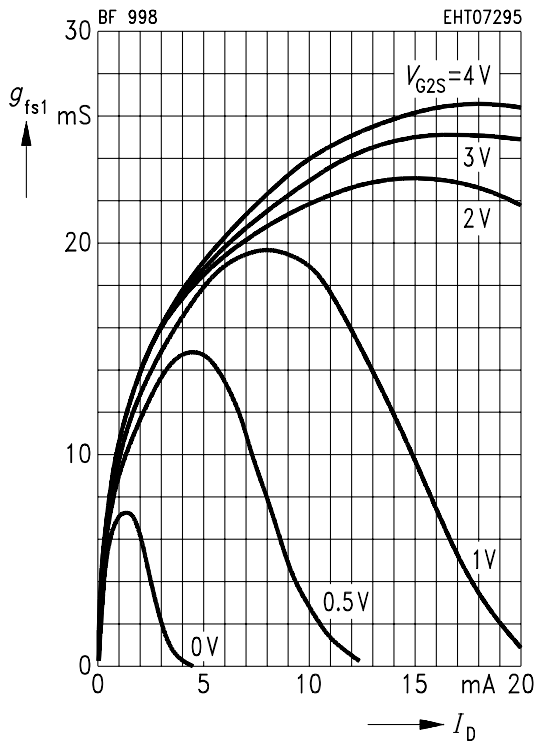
$V_{DS} = 8 \text{ V}, I_{DSS} = 10 \text{ mA}, f = 1 \text{ kHz}$



Gate 1 forward transconductance

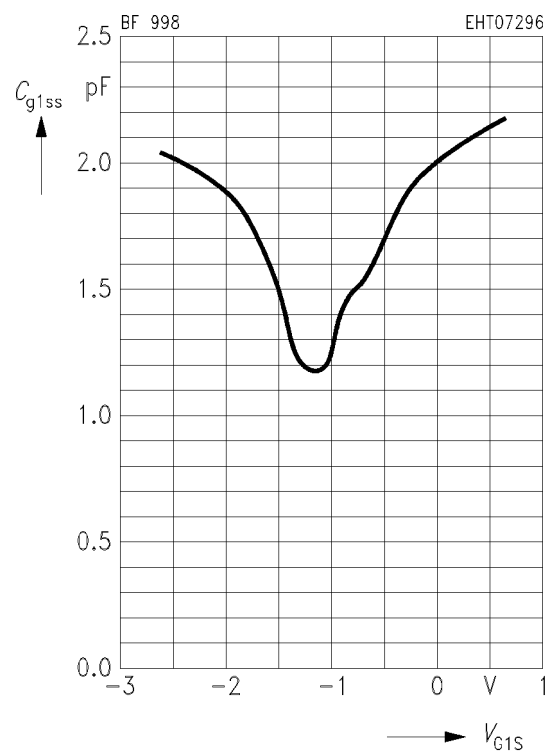
$g_{fs1} = f(I_D)$

$V_{DS} = 8\text{ V}, I_{DSS} = 10\text{ mA}, f = 1\text{ kHz}$



Gate 1 input capacitance $C_{g1ss} = f(V_{G1S})$

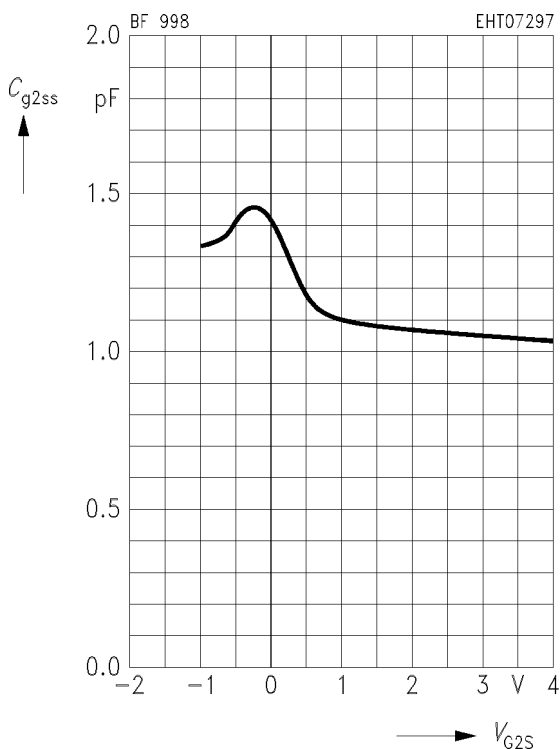
$V_{G2S} = 4\text{ V}, V_{DS} = 8\text{ V}, I_{DSS} = 10\text{ mA}, f = 1\text{ MHz}$



Gate 2 input capacitance $C_{g2ss} = f(V_{G2S})$

$V_{G1S} = 0\text{ V}, V_{DS} = 8\text{ V}$

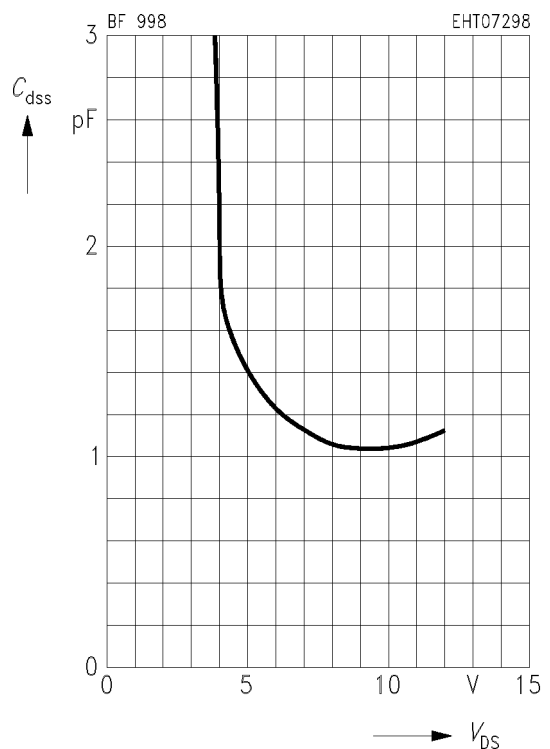
$I_{DSS} = 10\text{ mA}, f = 1\text{ MHz}$



Output capacitance $C_{dss} = f(V_{DS})$

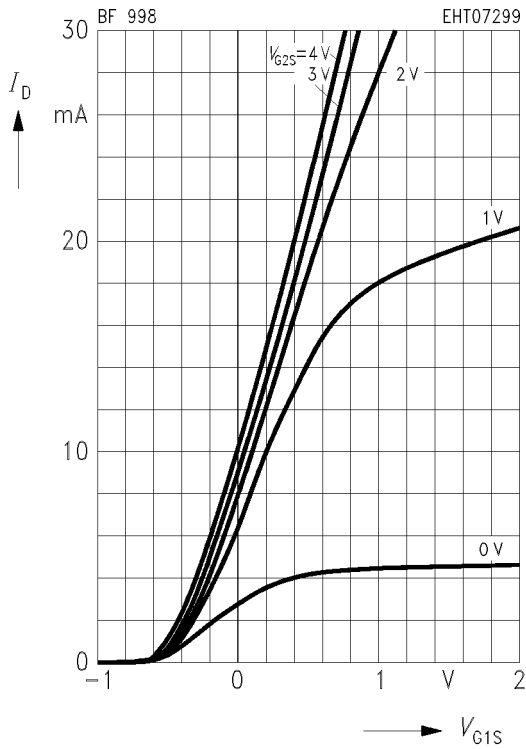
$V_{G1S} = 0\text{ V}, V_{G2S} = 4\text{ V}$

$I_{DSS} = 10\text{ mA}, f = 1\text{ MHz}$



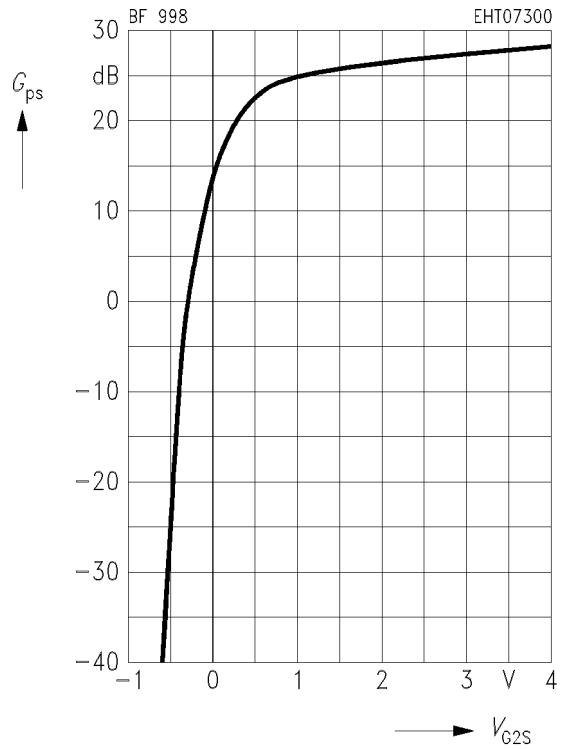
Drain current $I_D = f(V_{G1S})$

$V_{DS} = 8\text{ V}$



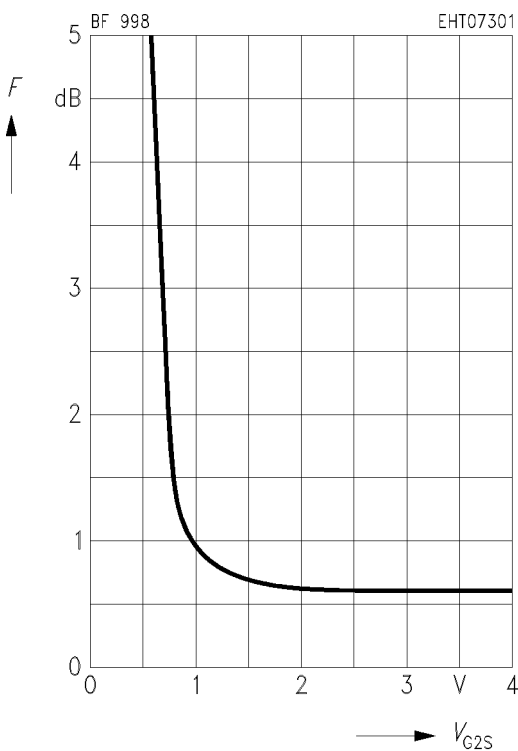
Power gain $G_{ps} = f(V_{G2S})$

$V_{DS} = 8\text{ V}, V_{G1S} = 0, I_{DSS} = 10\text{ mA}, f = 200\text{ MHz}$ (see test circuit 1)



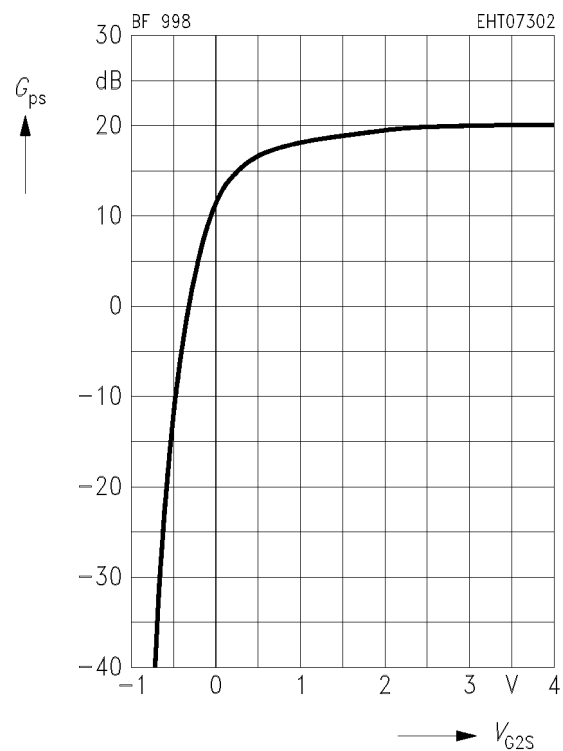
Noise figure $F = f(V_{G2S})$

$V_{DS} = 8\text{ V}, V_{G1S} = 0, I_{DSS} = 10\text{ mA}, f = 200\text{ MHz}$ (see test circuit 1)



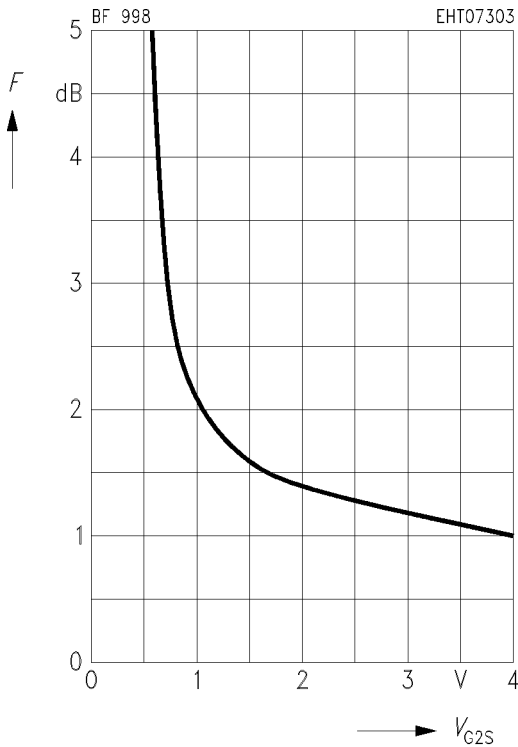
Power gain $G_{ps} = f(V_{G2S})$

$V_{DS} = 8\text{ V}, V_{G1S} = 0, I_{DSS} = 10\text{ mA}, f = 800\text{ MHz}$ (see test circuit 2)



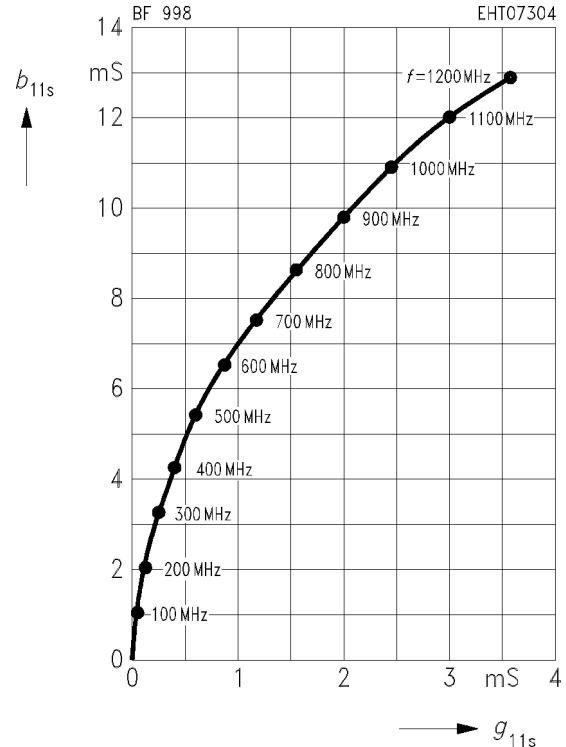
Noise figure $F = f(V_{G2S})$

$V_{DS} = 8\text{ V}$, $V_{G1S} = 0$, $I_{DSS} = 10\text{ mA}$,
 $f = 800\text{ MHz}$ (see test circuit 2)



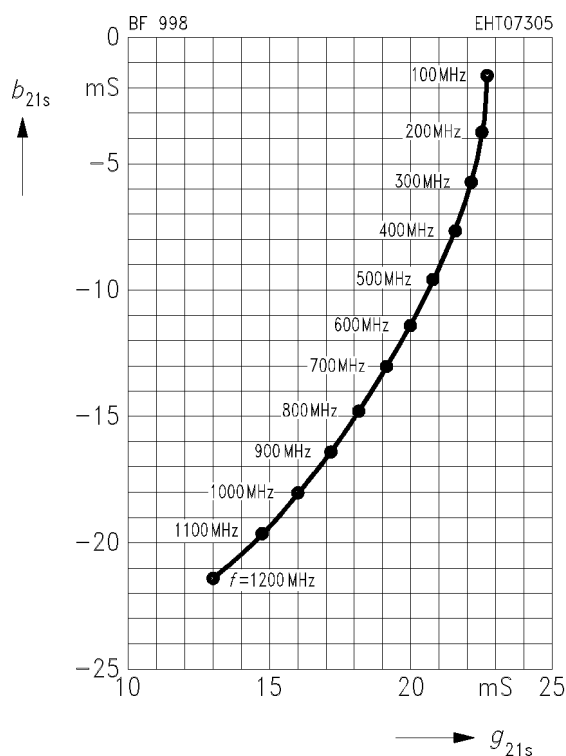
Gate 1 input admittance y_{11s}

$V_{DS} = 8\text{ V}$, $V_{G2S} = 4\text{ V}$, $V_{G1S} = 0$,
 $I_{DSS} = 10\text{ mA}$ (common-source)



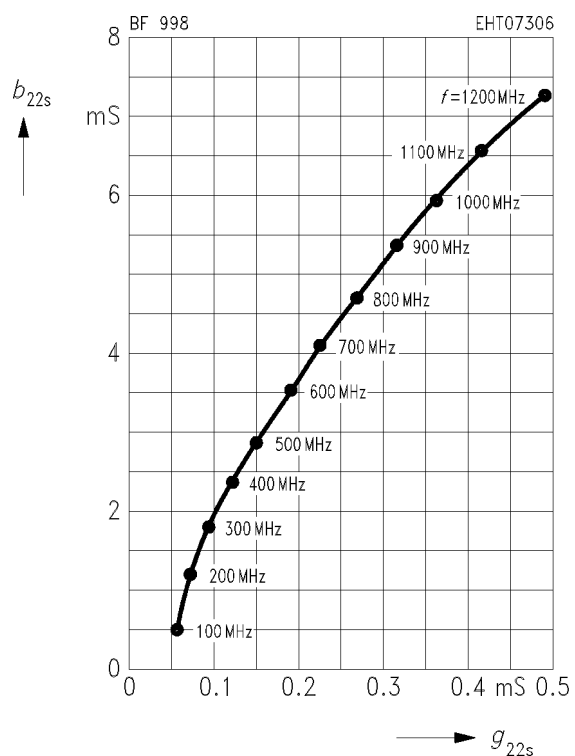
Gate 1 forward transfer admittance y_{21s}

$V_{DS} = 8\text{ V}$, $V_{G2S} = 4\text{ V}$, $V_{G1S} = 0$,
 $I_{DSS} = 10\text{ mA}$ (common-source)



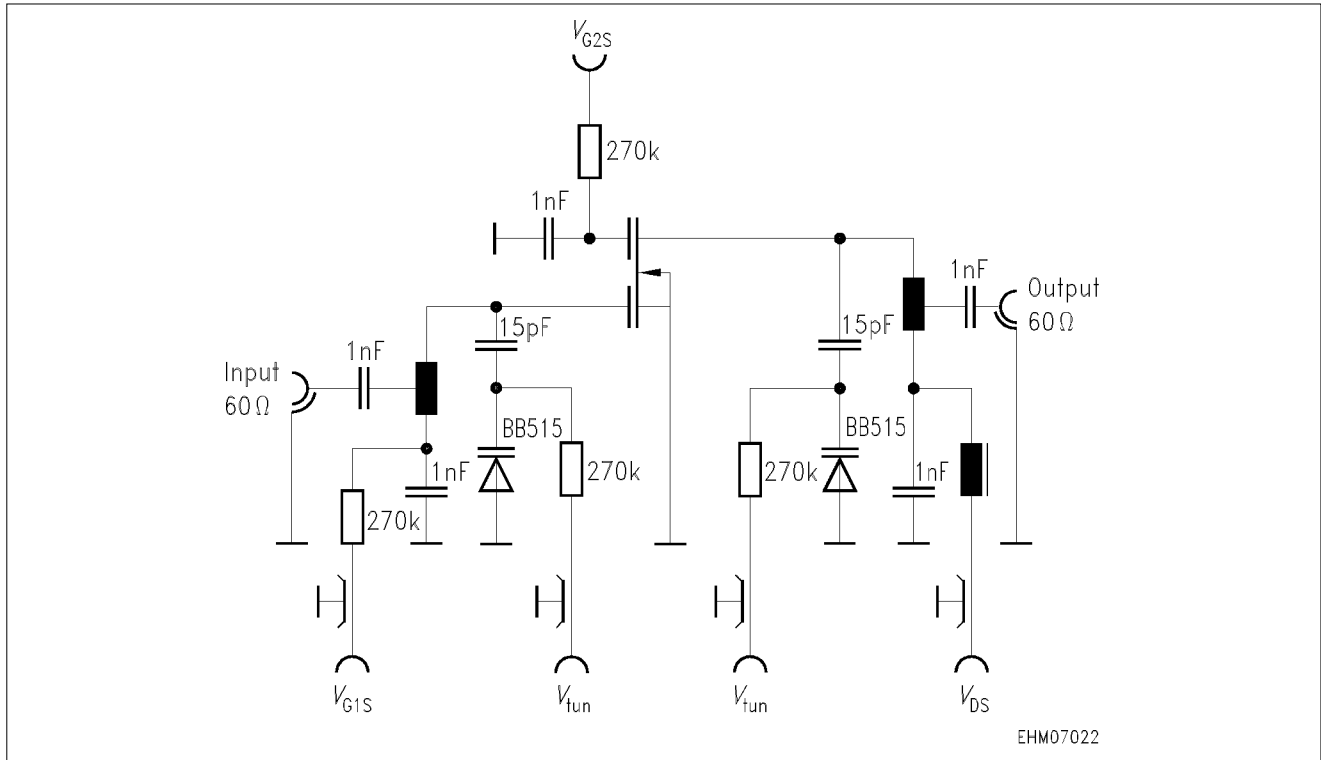
Output admittance y_{22s}

$V_{DS} = 8\text{ V}$, $V_{G2S} = 4\text{ V}$, $V_{G1S} = 0$,
 $I_{DSS} = 10\text{ mA}$ (common-source)



Test circuit 1 for power gain and noise figure

$f = 200 \text{ MHz}$, $G_G = 2 \text{ mS}$, $G_L = 0.5 \text{ mS}$



Test circuit 2 for power gain and noise figure

$f = 800 \text{ MHz}$, $G_G = 3.3 \text{ mS}$, $G_L = 1 \text{ mS}$

